

Cont
A5
a capacitor C_T having one terminal coupled to one terminal of the parasitic capacitance C_P and the other terminal coupled between a current source 12 and an NMOS transistor 14 having its gate coupled to its drain, as well as with the gate of the second NMOS transistor 16. A PMOS transistor 18 has its drain and gate coupled to a drain of NMOS transistor 16 as well as with the gate of the second PMOS transistor 20.

IN THE CLAIMS

Please amend claim 5 as follows:

A6
5. (Amended) Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:
a detection circuit for detecting a change in voltage of said input signal coupled to said input; and
a correction circuit coupled to said detection circuit for compensating for current from said input signal diverted to said parasitic capacitance due to a positive edge of said input signal.

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Please add the following new claims 18-25:

A7
--18. The method of claim 1 wherein the parasitic capacitance is across said input and ground, said introducing step including introducing the current to said input.

Sub B4
19. The method of claim 3 wherein the parasitic capacitance is across said input and ground, said introducing step including introducing the current to said input.

20. The apparatus of claim 9 wherein said parasitic capacitance appears between said input and ground.

21. The apparatus of claim 11 wherein said parasitic capacitance appears between said input and ground.

22. The apparatus of claim 12 wherein said parasitic capacitance appears between said input and ground.

Sub B3
23. The method of claim 13 wherein the parasitic capacitance is across said input and ground, said introducing step including introducing the current to said input.

AS
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